AMENDMENTS TO CLAIMS

1. (currently amended) A differential phase shift keying (DPSK) receiver to receive a DPSK input signal transmitted by a DPSK transmitter, comprising:

means for converting the input signal to in-phase and quadrature components;

a differential demodulator to determine a demodulated phase by comparing the in-phase and quadrature components of the input signal with a first delayed, conjugated version of the in-phase and quadrature components of the input signal;

a frequency offset calculation circuit to determine a frequency offset between an oscillator in the DPSK receiver and an oscillator in the DPSK transmitter by comparing the in-phase and quadrature components of the input signal with a second delayed, conjugated version of the in-phase and quadrature components of the input signal, wherein the delay associated with the second delayed, conjugated version of the in-phase and quadrature components of the input signal is ~~approximately~~ less than one ~~sample~~ symbol interval;

a frequency correction circuit to correct the demodulated phase using the frequency offset into a corrected phase;

a phase correction circuit to determine an absolute phase using the corrected phase; and

a symbol mapping circuit to map the absolute phase to an output symbol, comprising one or more bits of data.

2. (original) The DPSK receiver recited in claim 1, comprising a glitch filter to filter the frequency offsets to remove noise and glitches caused by phase transients between symbols.

3. (previously presented) The DPSK receiver recited in claim 1, wherein the delay associated with the first delayed version of the in-phase and quadrature components of the input signal in the differential demodulator is approximately one symbol interval.

4. (canceled)

5. (original) The DPSK receiver recited in claim 1, further comprising an optimal sample calculation circuit to determine an optimal sample to use to determine the demodulated phase and the frequency offset.

6. (original) The DPSK receiver recited in claim 5, wherein the optimal sample calculation circuit determines the optimal sample as the sample associated with a peak amplitude of the combined in-phase and quadrature components of each sample in each symbol interval.

7. (original) The DPSK receiver recited in claim 5, comprising a glitch filter to filter the frequency offsets to remove noise and glitches caused by phase transients between symbols.

8. (currently amended) A method for demodulating a differential phase shift keying (DPSK) input signal, comprising:

receiving the DPSK input signal;

digitizing the DPSK input signal;

converting the DPSK input signal into its corresponding in-phase (I) and quadrature (Q) components;

filtering the I and Q components of the DPSK input signal to remove noise;

determining a phase associated with the I and Q components of the DPSK input signal by comparing the I and Q components of the DPSK input signal to a first delayed and conjugated version of the I and Q components of the DPSK input signal;

determining a frequency offset associated with the I and Q components of the DPSK input signal by comparing the I and Q components of the DPSK input signal to a second delayed and conjugated version of the I and Q components of the DPSK input signal, wherein the delay associated with the second delayed and conjugated version of the I and Q components of the DPSK input signal is ~~approximately~~ less than one ~~sample~~ symbol interval;

adjusting the determined phase using the determined frequency offset;

converting the adjusted phase to an absolute phase; and

mapping the absolute phase to a symbol corresponding to one or more data bits.

9. (previously presented) The method recited in claim 8, wherein the step of determining the phase further comprises delaying the I and Q components of the DPSK input signal by approximately one symbol interval and reversing the sign of the Q component to generate the first delayed and conjugated version of the I and Q components of the DPSK input signal.

10. (previously presented) The method recited in claim 8, wherein the step of determining the frequency offset comprises delaying the I and Q components of the DPSK input signal by approximately one sample interval and reversing the sign of the Q component to generate the second delayed and conjugated version of the I and Q components of the DPSK input signal.

11. (original) The method recited in claim 8, further comprising removing glitches caused by phase transients between symbols.

12. (original) The method recited in claim 8, further comprising determining an optimal sample to use in the steps of the determining the phase and frequency offset.

13. (original) The method recited in claim 12, further comprising:

calculating an amplitude for each sample in a symbol interval; and

selecting the sample corresponding to the greatest amplitude as the optimal sample.

14. (original) The method recited in claim 12, further comprising removing glitches caused by phase transients between symbols.

15. (currently amended) A system for demodulating a differential phase shift keying (DPSK) input signal, comprising:

means for converting the DPSK input signal into its corresponding in-phase (I) and quadrature (Q) components;

means for filtering the I and Q components of the DPSK input signal to remove noise;

means for determining a phase associated with the I and Q components of the DPSK input signal by comparing the I and Q components of the DPSK input signal to a first delayed and conjugated version of the I and Q components of the DPSK input signal;

means for determining a frequency offset associated with the I and Q components of the DPSK input signal by comparing the I and Q components of the DPSK input signal to a second

delayed and conjugated version of the I and Q components of the DPSK input signal, wherein the delay associated with the second delayed and conjugated version of the I and Q components of the DPSK input signal is ~~approximately~~ less than one ~~sample~~ symbol interval;

means for adjusting the determine phase using the determined frequency offset;

means for converting the adjusted phase to an absolute phase; and

means for mapping the absolute phase to a symbol corresponding to one or more data bits.

16. (previously presented) The system recited in claim 15, further comprising means for delaying the I and Q components of the DPSK input signal by approximately one symbol interval and reversing the sign of the Q component to generate the first delayed and conjugated version of the I and Q components of the DPSK input signal.

17. (previously presented) The system recited in claim 15, further comprising means for delaying the I and Q components of the DPSK input signal by approximately one sample interval and reversing the sign of the Q component to generate the second delayed and conjugated version of the I and Q components of the DPSK input signal.

18. (original) The system recited in claim 15, further comprising means for removing glitches caused by phase transients between symbols.

19. (original) The system recited in claim 15, further comprising means for determining an optimal sample to use for determining the phase and frequency offset.

20. (original) The system recited in claim 19, further comprising:

means for calculating an amplitude for each sample in a symbol interval; and

means for selecting the sample corresponding to the greatest amplitude as the optimal sample.

21. (original) The system recited in claim 20, further comprising means for removing glitches caused by phase transients between symbols.

22. (new) The DPSK receiver recited in claim 1, wherein the delay associated with the second version of the in-phase and quadrature components of the input signal in the frequency offset calculation circuit is approximately one sample interval.